HyperTransport™ Technology Consortium

"Here and Now!"

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Briefing Agenda

- **HyperTransport ™ : "Here and Now!"**
  - Technology backgrounder
  - Enabling future I/O technologies
- **HyperTransport Technology Consortium overview**
- **New members announced**
- **HyperTransport applications**
  - Computer, communications, and embedded applications
  - Products available today
- **Developing future specifications & new markets**
- **Summary**

HyperTransport: Here and Now!

- **HyperTransport ™ technology improves overall system performance**
  - High-speed, high performance, point-to-point link for ICs
  - Enables chips inside PCs, networking and communications devices to communicate up to 48 times faster than some existing bus technologies
  - Provides 12.8 G byte/sec total bandwidth
- **HyperTransport buses have two unidirectional links**
  - Links can be 2-,4-,8-,16- or 32-bits wide in each direction
- **Products shipping now**

Enabling Future Technologies

- **Provides designers with clear, reliable upgrade path**
  - Supports existing PCI, AGP, 1394, USB 2.0, and 1Gigabit Ethernet bus interfaces
- **High-speed, low pin-count interconnect for emerging I/O connections**
  - PCI-X, PCI 3.0
  - InfiniBand
  - South Bridge
  - AGP 8x
  - 10Gigabit Ethernet

Consortium Background

- HyperTransport ™ Technology Consortium launched July 2001
- Members represent the networking, telecommunications and computer industries
- HyperTransport Technology Consortium Promoters:


HyperTransport Consortium's Goals

- Promote the adoption of HyperTransport™ technology as a "free" industry interconnect standard
- Drive the expansion of a HyperTransport infrastructure to benefit the companies who incorporate it
- Evolve HyperTransport technology for new applications, emerging requirements, and future manufacturing technologies
- Ensure compatibility and interoperability of HyperTransport enabled devices

HTC Welcomes New Members

ANNOUNCING 14 NEW MEMBERS:

0-In Design Automation, Acer Laboratories Inc., Altera, AMCC, Fast-Chip, Flow Engines, GDA Technologies, Josipa Company, LEDA Systems, Marvell Semiconductor, Nokia, Spinnaker Networks, Teradyne, Xilinx

- **Over 200 companies have evaluated the HyperTransport ™ I/O specification**

Membership Benefits

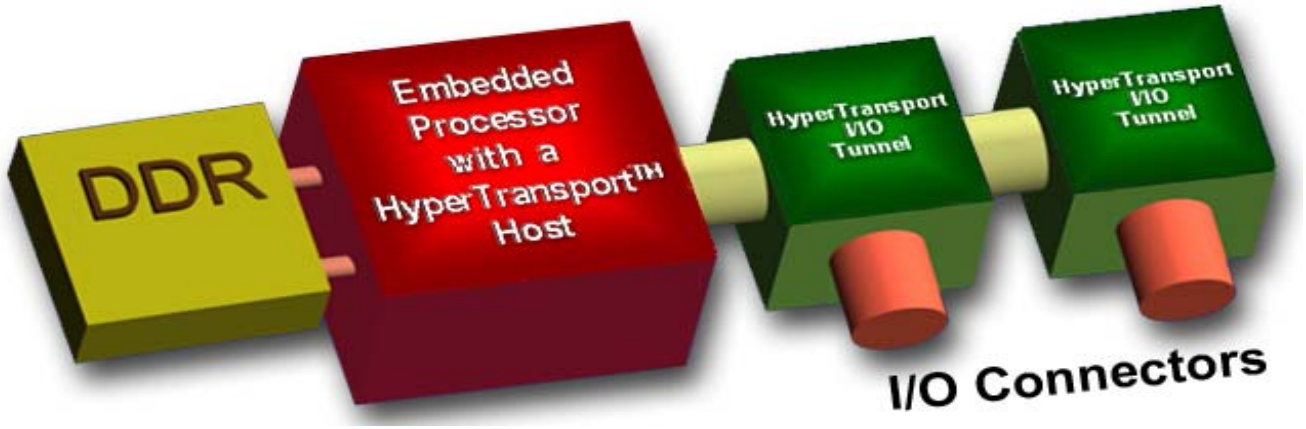
- **All members receive Royalty-free license to HyperTransport ™ I/O technology Intellectual Property (with payment of annual dues)**
- **Contributor Members**
  - May hold voting seats on Working Groups
  - May participate on Task Forces
  - Entitled to participate in Marketing events
  - Entitled to review preliminary and pre-released documents
- **Adopter Members**
  - Non-voting members
  - May participate in Task Forces

HyperTransport: Applications

- Microprocessors
- Routers
- Hubs
- Switches
- Servers
- Test equipment
- Workstations
- HDTV equipment
- PCs (desktop & notebook)
- Set-top boxes
- Mobile/handheld devices
- Game consoles
- Embedded systems

Any Application Requiring High Speed, Low Latency & Scalability!

Embedded Applications and I/O Tunnels



- **For the 1st time in the industry:**
  - I/O devices shared among computation and communication industry
  - Unique "TUNNELING" capability designed to provide almost unlimited I/O expandability
  - Fundamentally different microprocessor and memory controllers may be designed to use the very same I/O components
  - Pin count adjustable for the necessary bandwidth
  - Cost reduced due the the cumulative volume
  - Extended component life

HyperTransport: Here and Now

- PMC-Sierra announced RM9000x2™ integrated MIPS multiprocessor
- NVIDIA announced nForce chipset with integrated graphics
- Broadcom announced BCM1250 MIPS CPU
- API Networks introduced the industry's first HyperTransport-to-PCI bridge chip, the AP1011, and the first HyperTransport switch, AP4041
- AMD announced Hammer, 8th generation architecture for microprocessors
- Altera uses Hypertransport in APEX II devices
- Xilinx uses Hypertransport in Virtex®-II devices
- Teradyne announced HyperTransport testers

Technical Goals

- **Manage and evolve the specifications**
  - manage incident reports, clarifications, revision control, FAQs
  - extend the feature set, as needed:
    - » error management
    - » larger address spaces
    - » coherency
    - » enhance security
- **Build the HyperTransport ™ Infrastructure**
  - resources and technical libraries
  - tools, testers, diagnostics, etc.
  - licensable IP: Register Transistor Level (RTL), Physical Interfaces (PHYs), verification suites, etc.
- **Protect the investment of early adopters**
  - interoperability and backwards compatibility

“New” Market Opportunities

To augment the adoption of HyperTransport ™ technology, the Consortium will promote the development of:

- A diverse mix of CPU/platform architectures
- Classifiers
- Security Chips
- TCP Termination
- 1 Gigabit / 10 Gigabit Ethernet solutions
- InfiniBand
- Connectors and cables
- Test equipment and verification tools
- Software tools and diagnostics
- EDA solutions

Summary

- HyperTransport ™ technology enables chips inside PCs, networking and communications devices to communicate with each other up to 48 times faster than some existing technologies
- HyperTransport Technology Consortium welcomes Broadcom and SGI as Promoter Members and an additional 14 new member companies
- HTC's goal is to drive the development and adoption of HyperTransport technology for current and future applications
- Products with HyperTransport are available and under development HERE AND NOW!